

Design teams are getting crushed by complexity with the exponential growth of unique IPs in the modern, AI-enabled, SoC.

1000s
of IP CORES

With 1000's of IP cores in a single SoC, the challenge of connecting these together correctly the first time requires new thinking.

2M +
registers

Managing over 2 million registers requires significant manual effort to generate accurate designs.



Magillem Connectivity

Streamline and shorten the connectivity integration process with optimized automation.



Continuous integration with a robust, **automated SoC build** process ensures error-free connectivity.



Using a **single source of truth** environment, consistency and interoperability between the design flow steps is assured.



A proven **correct-by-construction** methodology, ensures high system quality.



Cut turnaround time from months to 3-4 weeks for initial builds or 3-4 weeks to 1-2 days for derivative designs.



Decrease integration errors and functional delays at the front-end by 30%.



Reduce team workload and turnaround time by up to 30%.



Save engineering resources, 3-5 engineers, per project.



Magillem Registers

Automate the hardware/software interface of the design.



Seamless integration for existing flows using solid APIs that allow customizable importer/exporter for memory map capture, updates and collateral generations.



Synchronized database between HW, SW, and documentation plus comprehensive consistency checks safeguards against misalignment.



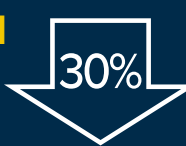
Reduce cycle time to completion with seamless integration in existing flows.



Gain weeks of time back, saving 35%+, shifting from 2-3 weeks to hours over manual processes.



Reduce manual errors and misalignments with a synchronized database.



Decrease errors by 30%+ leveraging up-to-date HSI information in various specialized formats for effective collaboration.

Magillem Design Flow

